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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/737,280	12/16/2003	Stephen M. Trimberger	X-1188 US	6162

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EXAMINER	
ABRAHAM, ESAW T	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 06/16/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/737,280	TRIMBERGER, STEPHEN M.	
	Examiner	Art Unit	
	Esaw T. Abraham	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-43* is/are pending in the application.

4a) Of the above claim(s) *10-23 and 32-43* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9 and 24-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/16/03*.
4) ☒ Interview Summary (PTO-413) Paper No(s)/Mail Date. *05/15/06* .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election / Restriction

Restriction to one of the following invention is required under 35 U.S.C. 121

Group I. Claims **1-9,** drawn to:

a) A method of utilizing a configurable random access memory (RAM) array in a programmable device, the RAM array comprising a user data portion and an error correction code (ECC) portion, the method comprising: receiving a user data word and a user address, the user data word having a selected virtual width; writing the user data word to a configurable subset of the user data portion of the RAM array, the configurable subset being determined by the selected virtual width. The user address; reading, while writing the user data word, from the RAM array at the user address a subset of a stored memory word, the stored memory word having a non-configurable width, the stored memory word including the user data word and the subset of the stored memory word; generating ECC data based on the user data word and the subset of the stored memory word; and writing the ECC data to the ECC portion of the RAM array at the user address (as in claim 1) classified in 714/763.

b) Claims **24-31**, drawn to:

A programmable structure comprising a configurable random access memory (RAM) circuit, the RAM circuit comprising: first and second sets of data lines; first and second sets of address lines; a first array of user data memory cells coupled to the first and second sets of data lines and further coupled to the first and second sets of

address lines; a second array of error correction code (ECC) memory cells coupled to the second set of data lines and the second set of address lines; a first write port coupled to the first sets of data and address lines, the first write port having a first plurality of configuration select input terminals, wherein the first write port stores user data in a configurable subset of the first array based on values supplied by the first plurality of configuration select input terminals; a second write port coupled to the second sets of data and address lines, wherein the second write port stores ECC data in the second array and further stores corrected data in the first and second arrays; a read port coupled to the first sets of data and address lines, the read port comprising a configurable select tree having a second plurality of configuration select input terminals, wherein the configurable select tree selects a configurable subset of data stored in the first array based on values supplied by the second plurality of configuration select input terminals; and an ECC generation and correction circuit coupled to the second sets of data and address lines and further coupled to provide the ECC data and the corrected data to the second write port (as in claim 24) classified in 714/763.

Group II. Claims **10-23** drawn to:

a) A method of utilizing a configurable random access memory (RAM) array in a programmable device, the RAM array comprising a user data portion and an error correction code (ECC) portion, the method comprising: receiving a user address; reading from the user address in the RAM array a memory word, the memory word comprising a user data word and ECC data, the user data word comprising a configurable subset of the memory word and having a selected virtual width; checking

the memory word read from the RAM array for at least one erroneous bit based on the ECC data included in the memory word; and providing a corrected version of the user data word as an output of the RAM array, the corrected version of the user data word having the selected virtual width (as in claim 11) is classified 714/758.

b) Claims **32-43** drawn to;

Programmable structure comprising a configurable random access memory (RAM) circuit, the RAM circuit comprising: a configurable array of memory cells, the array comprising a first portion storing user data and a second portion storing error correction code (ECC) data, the array having a read port and a first write port, the first portion having a configurable width; an ECC generation and correction circuit having a plurality of input terminals coupled to the read port of the array and a first plurality of output terminals; and a configurable select tree coupled to the first plurality of output terminals of the ECC generation and correction circuit (as in claim 32) is classified in 714/758.

The invention are distinct, each from the other because of the following reasons: Invention Group I and group II are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if they are shown to be separately usable.

In the instance case, invention Group I has separate utility separate utility such as receiving a user data word and a user address, writing the user data word to a user data portion of the RAM array; reading, while writing the user data word, from the RAM array at the user address a subset of a stored memory word, and generating ECC data

based on the user data word and writing the ECC data to the ECC portion of the RAM array at the user address and further a programmable structure comprising a configurable random access memory (RAM) circuit, the RAM circuit comprising: first and second sets of data lines; first and second sets of address lines; a first array of user data memory cells coupled to the first and second sets of data lines and further coupled to the first and second sets of address lines; a second array of error correction code (ECC) memory cells coupled to the second set of data lines and the second set of address lines.

In the instant case, the invention of Group II has separate utility such as a method comprising: receiving a user address; reading from the user address in the RAM array a memory word, the memory word comprising a user data word and ECC data, the user data word comprising a configurable subset of the memory word and having a selected virtual width; checking the memory word read from the RAM array for at least one erroneous bit based on the ECC data included in the memory word; and providing a corrected version of the user data word as an output of the RAM array, the corrected version of the user data word having the selected virtual width. See MPEP 806.05(d).

Because these inventions are distinct for the reason given above and the search required for Group I is not required for Group II, restriction for examination purposes as indicated is proper.

Because these inventions are distinct for the reason given above and the reasons given above and search required for Group II is not for Group I, restriction for examination purposes as indicated is proper.

Because these inventions are distinct for the reason given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

Because these inventions are distinct for the reasons given above and have acquired a separate status in the art because or their recognized divergent subject matter, restriction for examination purposes as indicated is proper.

During a telephone conversation with Lois Carther on 05/16/06 a provisional election was made with traverse to prosecute the invention of Group I, claims 1-9 and 24-31.

Applicant is advised that the reply to this requirement to be complete must include an election of the invention to be examined even though the requirement is traversed (37 CFR 1.143).

Applicant is reminded that upon cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the specification. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

DETAILED ACTION

1. Claims **1-9 and 24-31** are presented for examination.

Information Disclosure Statement

2. The references listed in the information disclosure statement submitted on 12/16/03 have been considered by the examiner (see attached PTO-1449).

Specification

3. The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U. S. C 112

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

4. Claims 1 and 24-31 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

a) As per claim 1, (lines 1, 7, 8, 13) "configurable, non-configurable" a positive term should be used.

b) As per claim 24, lines (1, 15, 23 and 25) "configurable" a positive term should be used.

c) As per claims 24-31, line 1, "programmable" a positive term should be used.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere* CO., 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. Claims **1-9** are rejected under 35 U.S.C. 103(a) as being unpatentable over Yada et al. (U.S. PN: 6,941,505) in view of McAlpine (U.S. PN: 6,167,491).

As per claim 1:

Yada et al. substantially teach or disclose in figure 7 teach a procedure used or executed when user data and ECC codes are written into their corresponding area

(20B) as other array data in association with one another. When an array of user data to be written is specified and a process for writing data with ECC codes is designated, the user data read. An array of user data is read into a memory as illustrated in FIG. 7(B) by way of example. Next, ECC codes are generated with respect to user data as illustrated in FIG. 7(A) by way of example and stored as another data array DA3 (S12). The writing of both data arrays DA1 and DA3 into the corresponding area 20Ba of the flash memory is carried out (S13 through S17). Write processing is similar to the procedure of Steps S4 through S7 referred to above (see col. 17, lines 54-67). Further, Yada et al. in figure 9 illustrates, as an example, a procedure executed when ECC code-added data in which the user data and ECC codes described in FIG. 7 are defined as discrete array data, are read. A leading address of the array data for the ECC codes intended for reading, and a leading address of the user data are first set (S31). An ECC code and user data corresponding to the leading addresses are read into a memory from each area 20Ba of the flash memory (S32). Further, an error decision is made to the read data (S33). Even when reference is made to the corresponding user data and ECC codes upon the error determination, information for specifying or designating their array's structures must be given through a user program (see col. 18, lines 20-42). **Not explicitly** described in the detail in the reference of Yada et al. is writing data to a memory (RAM) wherein the data determined by a selected width and an address. **However,** McAlpine teaches a single write descriptor (262) transfers all valid data to the RAM core (26) from the in queue registers (52) associated with the particular port (18) corresponding to the descriptor (262). In this transfer, the data is routed through the

multiplexer (152) and the position shifter (154). These elements provide for writing the valid data into the RAM array (56) starting at any column of an addressed row and the memory circuit (36) provides for placing in the RAM array (56) a block of data, the size of the block being independently selectable and the placement of the block in the RAM array (56) starting at an independently selectable position. In addition, the memory circuit (36) provides for storing various blocks of data at independently selectable positions in the RAM array (56) (see col. 24, lines 50-67). **Therefore,** it would have been obvious to a person having an ordinary skill in the art at the time the invention was made to incorporated the method of writing data to a RAM array by selecting size of data as taught by McAlpine into the invention of Yada et al. **This modification** would have been obvious because a person having ordinary skill in the art would have been motivated in order to provide a memory circuit capable of supporting ports of selectable word width while providing substantially unrestricted random accessibility to the memory through all ports, in variable size blocks and in both read and write operations (see col. 5, lines 32-39).

As per claims 2-3:

Most of the limitations of these claims have been noted in the rejection of claim 1. In addition McAlpine disclosed a single write descriptor 262 transfers all valid data to the RAM core 26 from the in queue registers 52 associated with the particular port (18) corresponding to the descriptor (262). In this transfer, the data is routed through the multiplexer 152 and the position shifter (154). These elements provide for writing the

valid data into the RAM array (56) starting at any column of an addressed row (see col. 24, lines 50-67).

As per claims 4-9:

Most of the limitations of these claims have been noted in the rejection of claim 1. In addition Yada et al. in figure 9 illustrates, as an example, a procedure executed when ECC code-added data in which the user data and ECC codes described in FIG. 7 are defined as discrete array data, are read. A leading address of the array data for the ECC codes intended for reading, and a leading address of the user data are first set (S31) (see col. 17, lines 54-67).

Allowable subject matter

6. Claims 24-31 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action.

Examiner's statement for reason for allowance

7. Claims **24-31** have been allowed.

The following is an examiner's statement for allowance:

The prior art of record (Yada et al.) (U.S. PN: 6,941,505) teach or disclose in figure 7 teach a procedure used or executed when user data and ECC codes are written into their corresponding area (20B) as other array data in association with one another. When an array of user data to be written is specified and a process for writing data with ECC codes is designated, the user data read. An array of user data is read into a memory as illustrated in FIG. 7(B) by way of example. Next, ECC codes are generated

with respect to user data as illustrated in FIG. 7(A) by way of example and stored as another data array DA3 (S12). The writing of both data arrays DA1 and DA3 into the corresponding area 20Ba of the flash memory is carried out (S13 through S17). Write processing is similar to the procedure of Steps S4 through S7 referred to above (see col. 17, lines 54-67). In addition, the prior art of record, McAlpine teaches a single write descriptor (262) transfers all valid data to the RAM core (26) from the in queue registers (52) associated with the particular port (18) corresponding to the descriptor (262). In this transfer, the data is routed through the multiplexer (152) and the position shifter (154). These elements provide for writing the valid data into the RAM array (56) starting at any column of an addressed row and the memory circuit (36) provides for placing in the RAM array (56) a block of data, the size of the block being independently selectable and the placement of the block in the RAM array (56) starting at an independently selectable position. However, the prior art taken singly or in combination fail to teach, anticipate, suggest, or render obvious a random access memory (RAM) circuit, the RAM circuit comprising: first and second sets of data lines; first and second sets of address lines; a first array of user data memory cells coupled to the first and second sets 'of data lines and further coupled to the first and second sets of address lines; a second array of error correction code (ECC) memory cells coupled to the second set of data lines and the second set of address lines; a first write port coupled to the first sets of data and address lines, the first write port having a first plurality of configuration select input terminals, wherein the first write port stores user data in a configurable subset of the first array based on values supplied by the first plurality of configuration select input

terminals; a second write port coupled to the second sets of data and address lines, wherein the second write port stores ECC data in the second array and further stores corrected data in the first and second arrays; a read port coupled to the first sets of data and address lines, the read port comprising a configurable select tree having a second plurality of configuration select input terminals, wherein the configurable select tree selects a configurable subset of data stored in the first array based on values supplied by the second plurality of configuration select input terminals; and an ECC generation and correction circuit coupled to the second sets of data and address lines and further coupled to provide the ECC data and the corrected data to the second write port. Consequently, claim 24s allowed over the prior art.

Claims **25-31** which is/are directly or indirectly dependent/s of claim 24 are also allowable over the prior art of record.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US PN: 6,253,299 Smith et al.

US PN: 6,662,334 Stenford, Ross J.

Any inquiry concerning this communication or earlier communication from the examiner should be directed to Esaw Abraham whose telephone number is (571) 272-3812. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are successful, the examiner's supervisor, Albert DeCady can be reached on (571) 272-3819. The fax phone numbers for the organization where this application or proceeding is assigned are (571) 273-8300 for regular communications and (571) 273-8300 for after final communications.

Information regarding the status of an Application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or PUBLIC PAIR. Status information for unpublished applications is available through Private Pair only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Esaw Abraham

Art unit: 2133

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